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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,876	11/26/2003	Ming-Jiunn Lai	LAIM 3007/EM	6015

34283 7590 07/14/2006

QUINTERO LAW OFFICE
1617 BROADWAY, 3RD FLOOR
SANTA MONICA, CA 90404

EXAMINER	
LUM, LEON YUN BON	

ART UNIT	PAPER NUMBER
1641	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,876	LAI ET AL.	
	Examiner	Art Unit	
	Leon Y. Lum	1641	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *April 20, 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *1-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed April 20, 2006 is acknowledged and has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 25-26 and 28-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al (US 2005/0056828 A1) in view of Snow et al (US 6,482,639 B2).

Wada et al reference teaches a MOS field effect transistor with a gate electrode 2 (i.e. bottom gate), a source electrode 4 (i.e. source), a drain electrode 5 (i.e. drain), and a channel layer 6 (i.e. nano channel layer), wherein the gate electrode is on a silicon substrate 1 (i.e. positioned on the silicon substrate), and the silicon substrate is layered with a gate insulating film 3 made of silicon oxide (i.e. gate dielectric layer; SiO_2 deposited on silicon substrate). See page 7, sections 0087-0092; and Figures 1A-C. Furthermore, Wada et al teach that the source electrode 4 and drain electrode 5 are placed over the channel layer 6 and different portions of the gate insulating film 3 (i.e. drain and source positioned extending over a first and second portion of a top surface of the nano channel layer and a first and second portion of a top surface of the gate dielectric layer, respectively). See page 9, section 0114 and Figure 2B.

However, Wada et al fail to teach a ceiling gate dielectric layer positioned on the drain and the source, comprising a first ceiling gate dielectric layer and a second ceiling gate dielectric layer, a ceiling gate positioned on the ceiling gate dielectric layer, a first protection layer positioned on the surface of the first ceiling gate dielectric layer, a

second protection layer positioned on the surface of the second ceiling gate dielectric layer, wherein the first protection layer, the second protection layer, and the first ceiling gate dielectric layer, the second ceiling gate dielectric layer and the nano channel layer are used to define a detection area for detecting an object so as to achieve the object of detecting the specific bio species for biomeasurement.

Snow et al reference teaches layers 60 and 70 comprising SiO_2 and Si_3N_4, respectively (i.e. ceiling gate dielectric layer), electrode 50 (i.e. ceiling gate; metal), and layer 80 comprising SiO_2 (i.e. protection layer), in order to perform molecular recognition using label-free assay techniques capable of real-time analysis, has high sensitivity, high resolution, and is cost-effective. See column 1, lines 60-63; column 3, line 56 to column 4, line 3; column 5, lines 18-35; and Figure 1. Since the layer and electrode embodiments are separated by active sensing region 110, each of the embodiments are separately on top of source 12 and drain 14. The layers and electrode on top of the source are therefore considered to read on "first ceiling gate dielectric", "first ceiling gate", and "first protection layer", and the layers and electrode on top of the drain are considered to read on "second ceiling gate dielectric", "second ceiling gate", and "second protection layer".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Wada et al with layers 60 and 70 comprising SiO_2 and Si_3N_4, respectively (i.e. ceiling gate dielectric layer; silicon oxide, silicon nitride), electrode 50 (i.e. ceiling gate), and layer 80 (i.e. protection layer), as taught by Snow et al, in order to perform molecular recognition using label-free assay techniques capable

of real-time analysis, has high sensitivity, high resolution, and is cost-effective. The layers and electrodes of Snow et al have the advantage of providing a means to detect analytes without labels, thereby providing motivation to combine the layers and electrodes of Snow et al with the device of Wada et al. In addition, one of ordinary skill in the art at the time of the invention would have had reasonable expectation of success in including the embodiments of Snow et al, in the device of Wada et al, since Wada et al teach a MOS field effect transistor, and the embodiments of Snow et al are also elements within a field effect transistor. Furthermore, the device of Wada et al provides a conducting path between the source and drain electrodes (see page 3, section 0049), and the layers of Snow et al isolate the source and drain from the substrate and protect them from the solution (see column 3, line 64 to column 4, line 1).

With respect to claim 26, Wada et al teach that gate 2 is polysilicon. See page 7, section 0091.

With respect to claim 33, Snow et al teach that electrode 50 covers both layers 60 and 70 (i.e. ceiling gate is any position on the ceiling gate dielectric layer). In addition, since the layers and electrode of Snow et al would completely cover the source and drain electrodes of Wada et al, the channel of Wada et al would necessarily be covered by the elements of Snow et al (i.e. ceiling gate covers a portion of the nano channel layer).

With respect to claims 34-35, Snow et al teach an array of sensors fabricated into a common substrate, wherein the sensors operate in parallel (i.e. plurality of double

nano gate device transistors connected to form a serial connection structure). See column 2, lines 42-48; and column 5, lines 22-24.

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al (US 2005/0056828 A1) in view of Snow et al (US 6,482,639 B2) as applied to claim 25 above, and further in view of Tsuruta et al (US 5,066,582).

Wada et al and Snow et al references have been disclosed above, and Snow et al additionally teaches that antibodies are immobilized on the FET. See column 5, lines 1-7. However, Wada et al and Snow et al fail to teach that a surfactant is absorbable on the nano channel layer.

Tsuruta et al reference teaches surfactants to wash the binding region on a substrate, in order to provide a blocking means on the substrate. See column 8, lines 56-63.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Wada et al and Snow et al with surfactants to wash the binding region on a substrate, as taught by Tsuruta et al, in order to provide a blocking means on the substrate. The surfactants of Tsuruta et al provide the advantage of preventing non-specific binding of biomolecules onto the binding region of a substrate, thereby increasing the substrate's binding effectiveness and providing motivation to combine the surfactants with the device of Wada et al and Snow et al. In addition, one of ordinary skill in the art at the time of the invention would have had reasonable expectation of success in including the surfactants of Tsuruta et al, in the device of

Wada et al and Snow et al, since Wada et al and Snow et al teach binding regions on a substrate, and the surfactants of Tsuruta et al are applied to binding regions.

Response to Arguments

7. On pages 9-11 of the Remarks, filed April 20, 2006, Applicants traverse the obviousness rejections in the previous Office Action. Specifically, Applicants argue two points:

(1) Applicants contend that Wada and Snow fail to teach limitations "a drain positioned extending over a first portion of a top surface of the nano channel layer and a first portion of a top surface the gate dielectric layer" and "a source position extending over a second portion of the top surface of the nano channel layer and a second portion of the top surface of the gate dielectric layer" in claim 25 since the channel layer 6 of Wada is formed over source and drain electrodes 4 and 5, respectively, or between the electrodes. See page 10, 3rd paragraph.

(2) Applicants allege that Snow does not teach the claimed ceiling gate of claim 25 since Snow explicitly teaches a "gateless" FET. See page 10, last paragraph.

Applicants' arguments have been fully considered, but are not considered persuasive. With respect to Applicants' first point (1) above, Wada actually teaches multiple embodiments of the MOS field effect transistor, including the embodiment

featured in Figure 2B, and described on page 9, section 0114. In this particular embodiment, it is clear that the source electrode 4 and drain electrode 5 are placed on top of the channel layer 6, and that each electrode is positioned over different portions of the gate insulating film 3. By being placed on top of the nano channel layer 6, the source electrode 4 and drain electrode 5 are considered to read on the limitations "extending over a first portion" and "extending over a second portion", respectively, "of the nano channel layer". In addition, since the electrodes are separated laterally, they necessarily extend over "a first portion" and "a second portion" of "the top surface the gate dielectric layer". Wada reference therefore clearly teaches the very limitation that Applicants allege is missing from the reference.

With respect to Applicants' second point (2) above, Snow defines the term "gate" as a "conductive layer" in the sentence directly preceding the sentence that Applicants cite in support of their argument. See column 3, lines 25-26. It is important to note that Snow discloses a "gateless" FET only in the context that there is no gate above the active channel. See column 3, lines 24-28. However, this situation is not claimed in the instant application. Electrode 50 (i.e. ceiling gate) meets Snow's definition of a "gate" and is applied in a situation totally different from the embodiment that describes Snow's "gateless" FET. Therefore, electrode 50 can still act as a "gate" since it is not above the active channel. When combined with Wada, the electrode has the advantage of allowing highly sensitive and cost-effective analyte detection on the MOS field effect transistor, thereby providing motivation to properly combine Wada and Snow references.

In light of the above arguments, Applicants' arguments are not considered persuasive and the rejections made in the previous Office Action are maintained.

Conclusion

8. No claims are allowed.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Y. Lum whose telephone number is (571) 272-2878. The examiner can normally be reached on weekdays from 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Long Le can be reached on (571) 272-0823. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leon Y. Lum
Patent Examiner
Art Unit 1641

LONG V. LE 07/26/06
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1600

LYL